UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,941,415 B1
APPLICATION NO. : 09/641519
DATED : September 6, 2005
INVENTOR(S) : Kevin J. Ryan

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title page should be deleted and substitute therefore the attached title page as shown on the attached page.

Drawings:

Delete drawing sheets 1-7, and substitute therefore the drawing sheets, consisting of Figs. 1-7, as shown on the attached pages.

Claim 20, column 9, line 30, "Link" should read --link--.

Signed and Sealed this

Tenth Day of October, 2006

Jon W. Dudas

JON W. DUDAS
Director of the United States Patent and Trademark Office

US006941415B1

(12) **United States Patent**
Ryan

(10) Patent No.: **US 6,941,415 B1**
(45) Date of Patent: **Sep. 6, 2005**

(54) **DRAM WITH HIDDEN REFRESH**

(75) Inventor: **Kevin J. Ryan**, Eagle, ID (US)

(73) Assignee: **Micron Technology, Inc.**, Boise, ID (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 274 days.

(21) Appl. No.: **09/641,519**

(22) Filed: **Aug. 21, 2000**

(51) **Int. Cl.**[7] **G06F 12/00**
(52) **U.S. Cl.** **711/106; 711/167; 711/168**
(58) **Field of Search** 711/104, 105, 711/100, 167, 168; 305/222, 189.01, 200, 193

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,172,282 A	* 10/1979	Aichelmann et al.	....	365/222
4,601,018 A	* 7/1986	Baum et al.	....	365/200
4,807,289 A	* 2/1989	Nakajima	....	704/251
4,849,936 A	* 7/1989	Mizutani	....	365/189.01
5,638,529 A	* 6/1997	Yee et al.	....	711/106
5,651,131 A	* 7/1997	Chesley	....	711/106
5,802,555 A	* 9/1998	Shigeeda	....	365/193
RE36,180 E	4/1999	Lim	....	365/189.04
5,959,923 A	* 9/1999	Matteson et al.	....	365/222
5,999,474 A	* 12/1999	Leung et al.	....	365/222
6,028,804 A	2/2000	Leung	....	365/222
6,167,484 A	* 12/2000	Boyer et al.	....	365/222
6,415,353 B1	* 7/2002	Leung	....	711/106

OTHER PUBLICATIONS

"MoSys Explains 1T-SRAM Technology," by Peter N. Glaskowsky, Microprocessor Report, vol. 13, No. 12, Sep. 13, 1999.

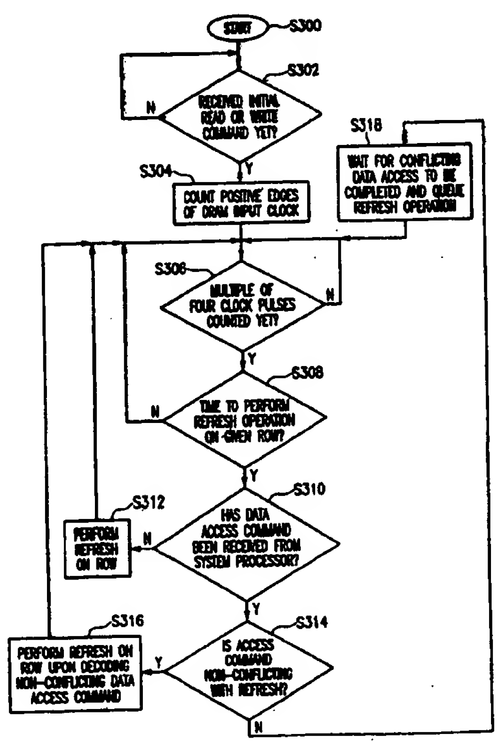
* cited by examiner

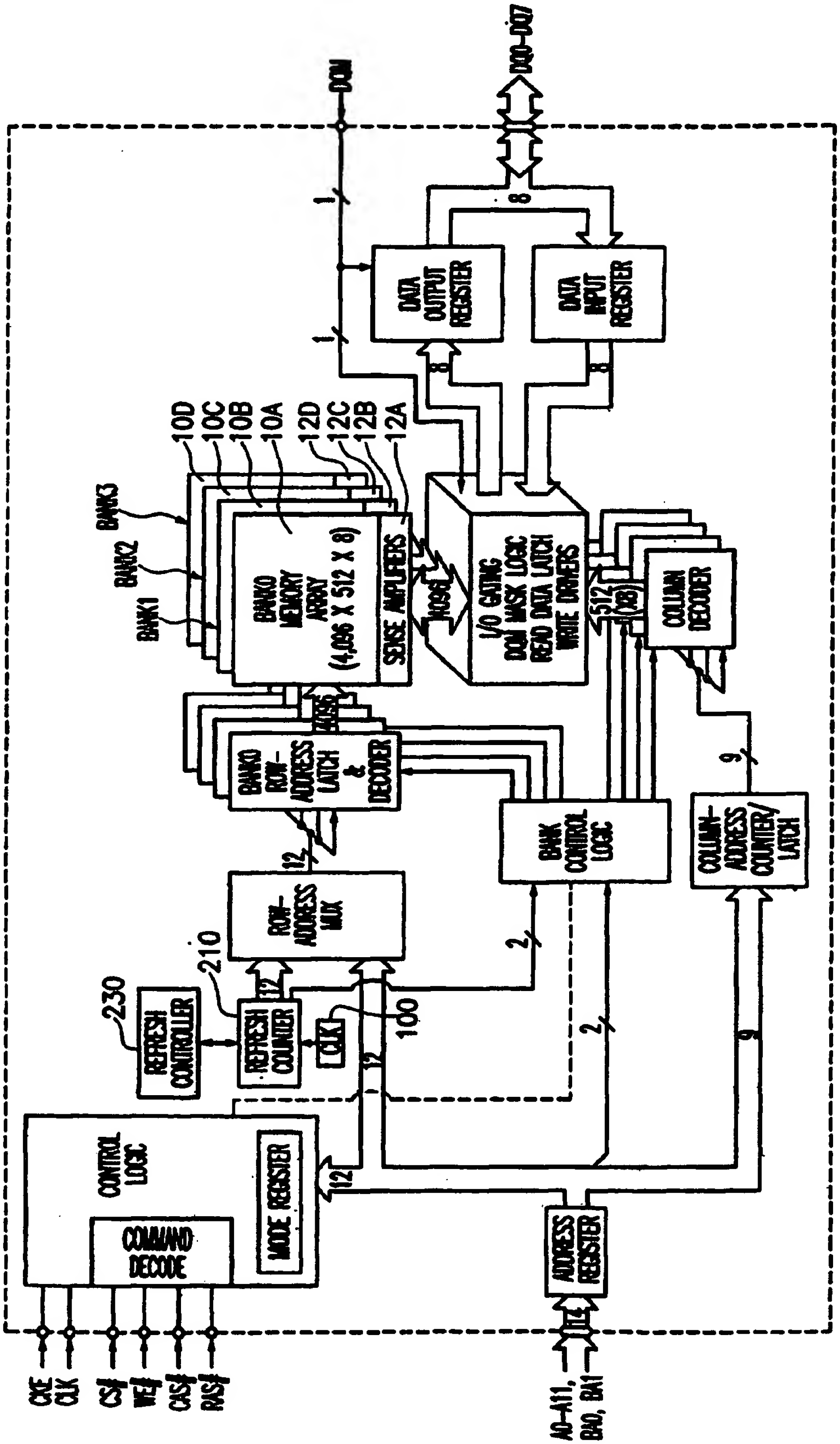
Primary Examiner—Brian R. Peugh
(74) *Attorney, Agent, or Firm*—Dickstein Shapiro Morin & Oshinsky LLP

(57) **ABSTRACT**

A synchronous DRAM is provided having specified time slots (e.g., every multiple of 4 clock pulses of a DRAM input clock) within which read or write commands may be entered on the command/address bus. During operation, the DRAM performs internally generated refresh operations on a periodic basis while avoiding collisions with controller-generated data accesses. An internal refresh cycle can be executed without interfering with any data accesses by starting the refresh after decoding a non-conflicting command in one of these time slots and finishing before the next command time slot. If an internal refresh operation is delayed (e.g., by the decoding of a conflicting access command) it will be completed at the earliest opportunity thereafter.

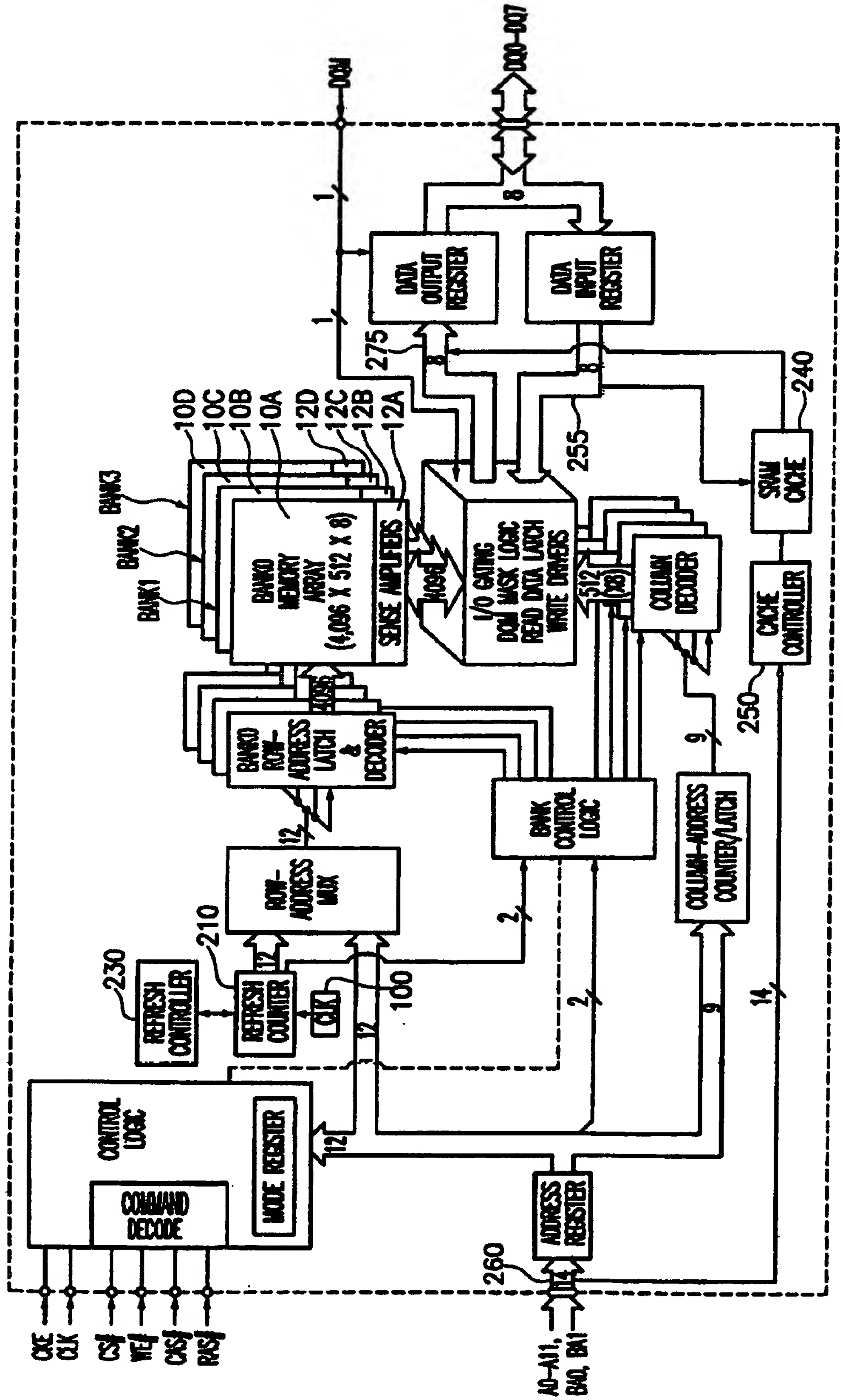
37 Claims, 7 Drawing Sheets





CKE
CLK
CS#
WE#
CAS#
RAS#
CONTROL LOGIC
COMMAND DECODE
MODE REGISTER
A0–A11, BA0, BA1
ADDRESS REGISTER
REFRESH CONTROLLER
230
210
REFRESH COUNTER
CLK
100
ROW-ADDRESS MUX
BANK0 ROW-ADDRESS LATCH & DECODER
4096
BANK CONTROL LOGIC
COLUMN-ADDRESS COUNTER/LATCH
BANK0 MEMORY ARRAY (4,096 X 512 X 8)
SENSE AMPLIFIERS
BANK1
BANK2
BANK3
10A
10B
10C
10D
12A
12B
12C
12D
I/O GATING DQM MASK LOGIC READ DATA LATCH WRITE DRIVERS
COLUMN DECODER
512 (x8)
DATA OUTPUT REGISTER
DATA INPUT REGISTER
DQM
DQ0–DQ7
12
2
9
8
1

FIG. 1



DQM
DQ0–DQ7
DATA OUTPUT REGISTER
DATA INPUT REGISTER
BANK0 MEMORY ARRAY (4,096 X 512 X 8)
SENSE AMPLIFIERS
I/O GATING DQM MASK LOGIC READ DATA LATCH WRITE DRIVERS
COLUMN DECODER
SRAM CACHE
CACHE CONTROLLER
BANK0 ROW-ADDRESS LATCH & DECODER
ROW-ADDRESS MUX
BANK CONTROL LOGIC
COLUMN-ADDRESS COUNTER/LATCH
REFRESH CONTROLLER
REFRESH COUNTER
CLK
CONTROL LOGIC
COMMAND DECODE
MODE REGISTER
ADDRESS REGISTER
BANK1
BANK2
BANK3
10A
10B
10C
10D
12A
12B
12C
12D
100
210
230
240
250
255
260
275
CKE
CLK
CS#
WE#
CAS#
RAS#
A0–A11, BA0, BA1

FIG. 2

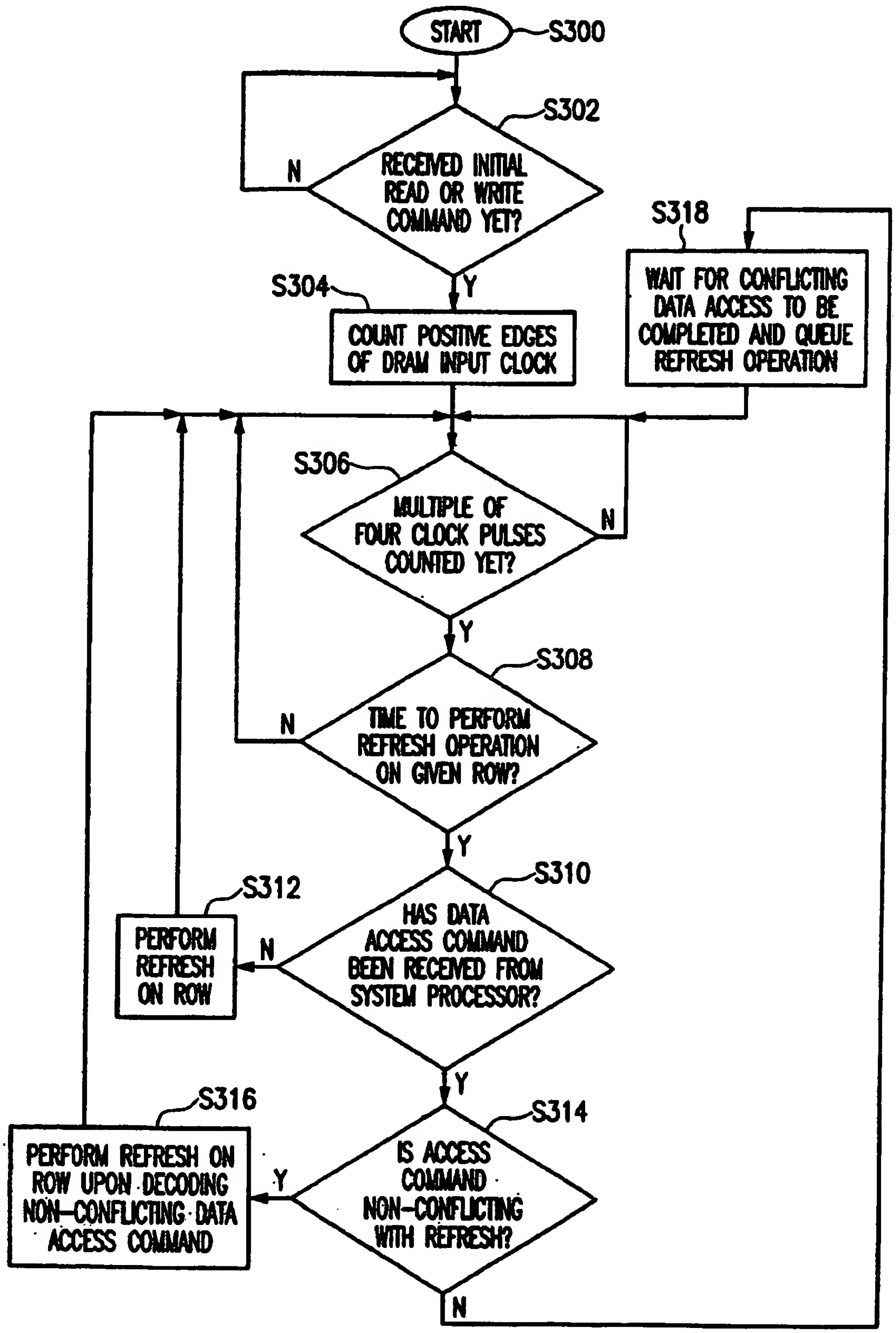

START
S300
S302
RECEIVED INITIAL READ OR WRITE COMMAND YET?
N
Y
S304
COUNT POSITIVE EDGES OF DRAM INPUT CLOCK
S318
WAIT FOR CONFLICTING DATA ACCESS TO BE COMPLETED AND QUEUE REFRESH OPERATION
S306
MULTIPLE OF FOUR CLOCK PULSES COUNTED YET?
N
Y
S308
TIME TO PERFORM REFRESH OPERATION ON GIVEN ROW?
N
Y
S310
HAS DATA ACCESS COMMAND BEEN RECEIVED FROM SYSTEM PROCESSOR?
S312
PERFORM REFRESH ON ROW
N
Y
S314
IS ACCESS COMMAND NON-CONFLICTING WITH REFRESH?
S316
PERFORM REFRESH ON ROW UPON DECODING NON-CONFLICTING DATA ACCESS COMMAND
Y
N

FIG. 3

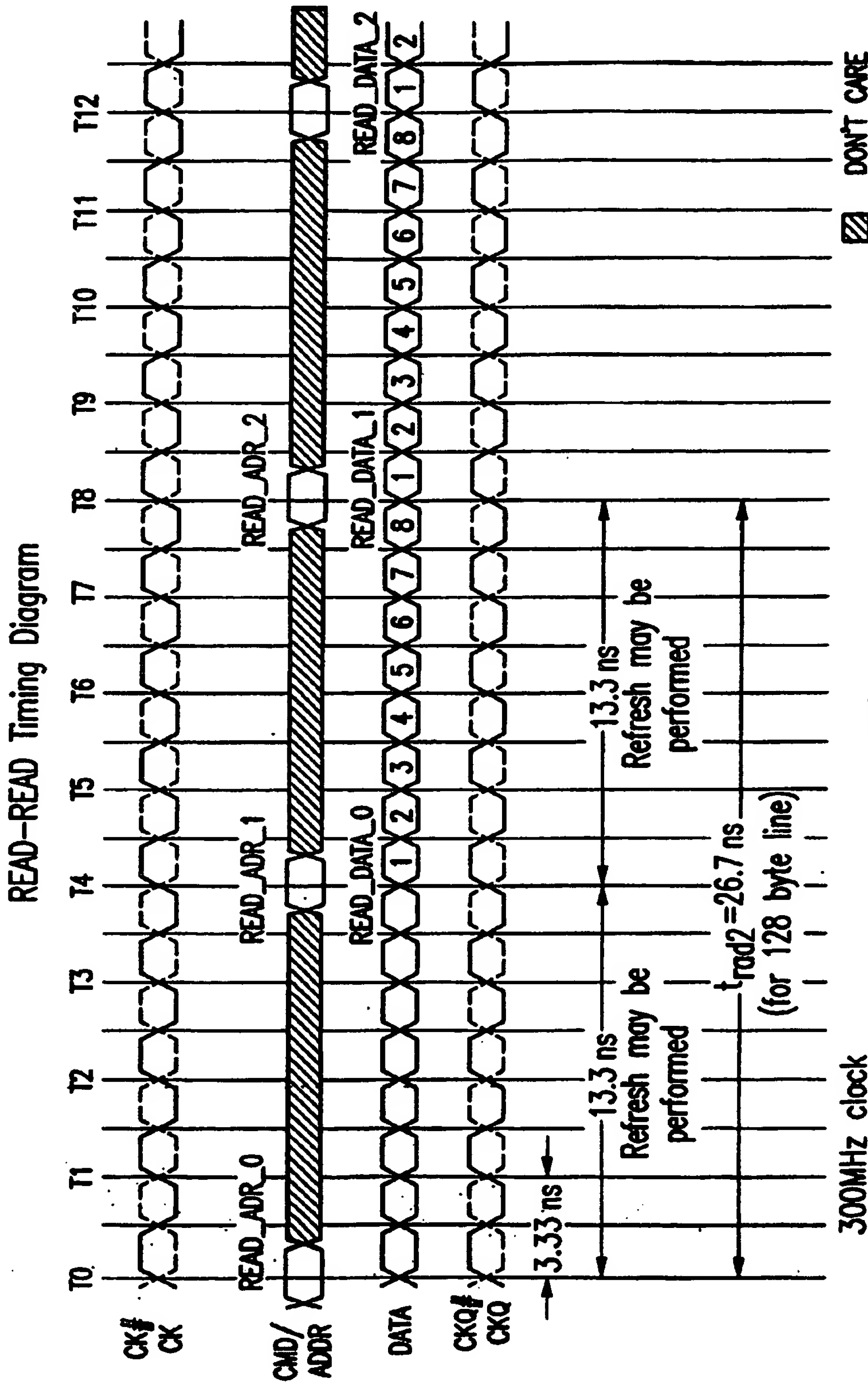

READ–READ Timing Diagram
T0
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
T11
T12
CK#
CK
CMD/
ADDR
DATA
CKQ#
CKQ
READ_ADR_0
READ_ADR_1
READ_ADR_2
READ_DATA_0
READ_DATA_1
READ_DATA_2
1 2 3 4 5 6 7 8
1 2 3 4 5 6 7 8
1 2
3.33 ns
13.3 ns
Refresh may be performed
13.3 ns
Refresh may be performed
t_{rad2}=26.7 ns
(for 128 byte line)
300MHz clock
DON'T CARE

FIG. 4

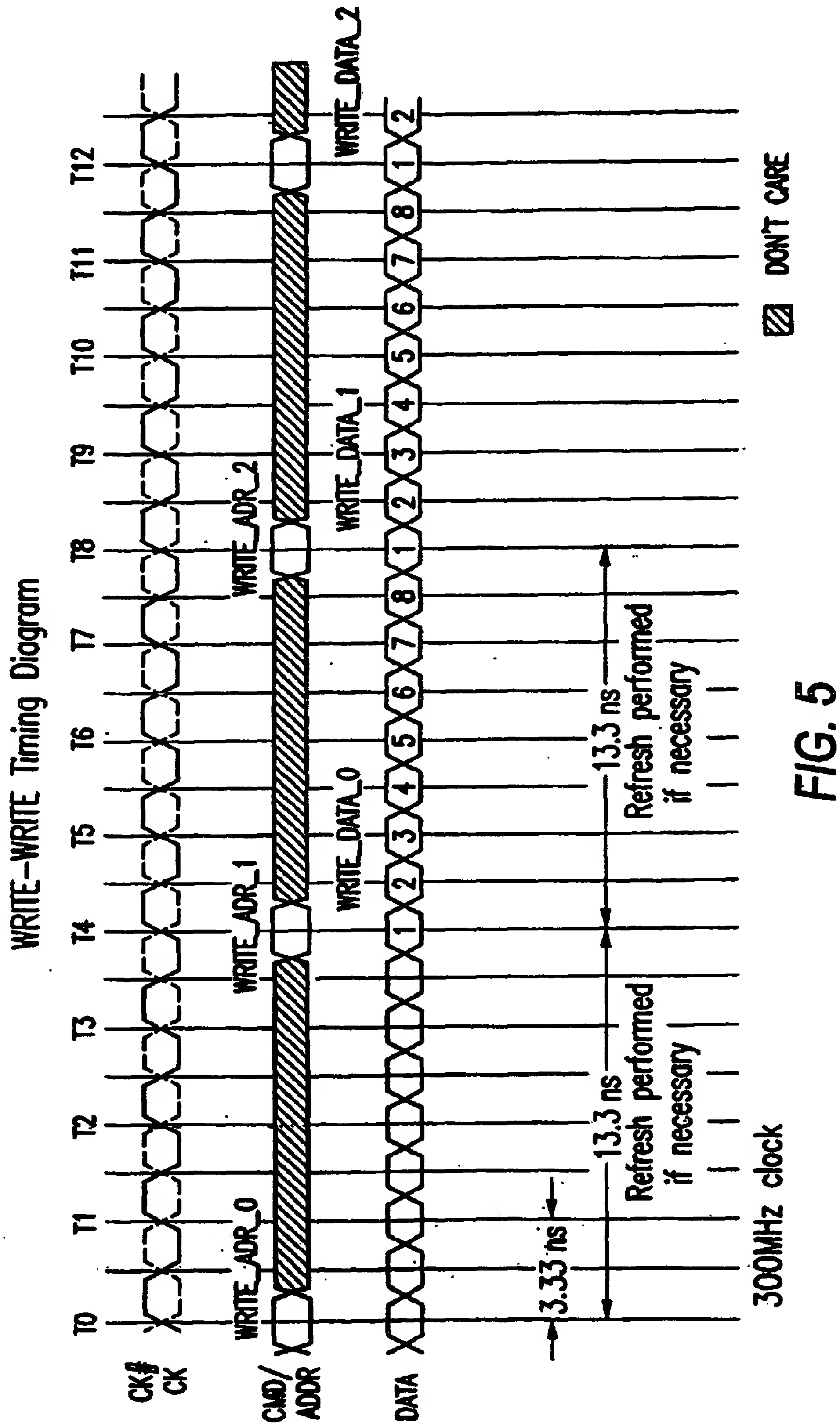

WRITE—WRITE Timing Diagram
T0
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
T11
T12
CK#
CK
CMD/
ADDR
DATA
WRITE_ADR_0
WRITE_ADR_1
WRITE_ADR_2
WRITE_DATA_0
WRITE_DATA_1
WRITE_DATA_2
3.33 ns
13.3 ns
Refresh performed
if necessary
13.3 ns
Refresh performed
if necessary
300MHz clock
DON'T CARE

FIG. 5

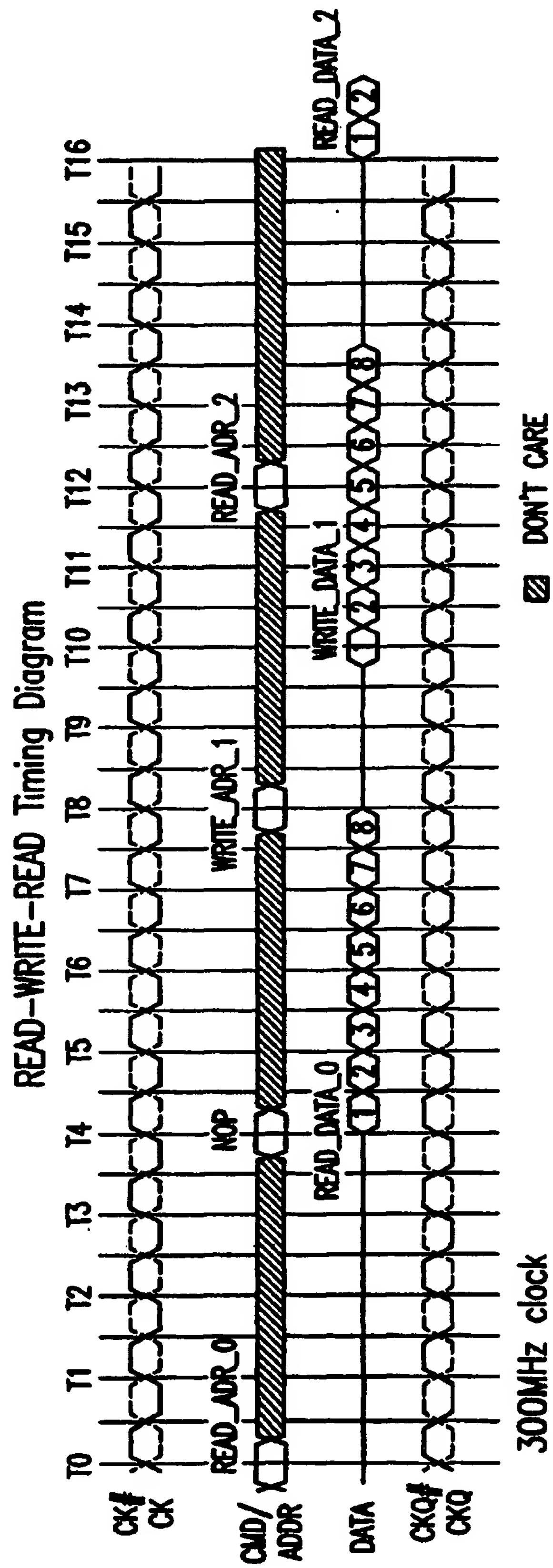

READ–WRITE–READ Timing Diagram
T0
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
T11
T12
T13
T14
T15
T16
CK#
CK
CMD/
ADDR
DATA
CKQ#
CKQ
READ_ADR_0
NOP
WRITE_ADR_1
READ_ADR_2
READ_DATA_0
WRITE_DATA_1
READ_DATA_2
1
2
3
4
5
6
7
8
300MHz clock
DON'T CARE

FIG. 6

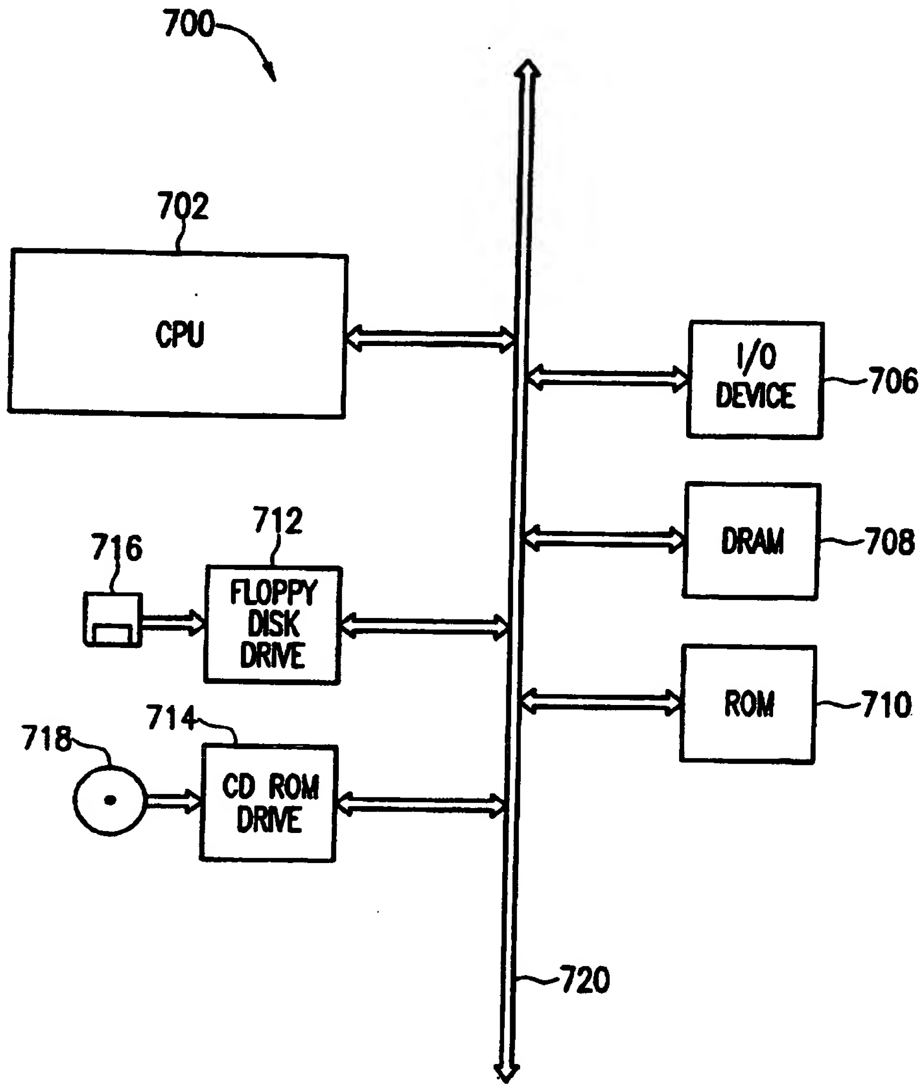

700
702
CPU
I/O DEVICE
706
DRAM
708
ROM
710
712
716
FLOPPY DISK DRIVE
714
718
CD ROM DRIVE
720

FIG. 7